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Richard Thomas Plunkett

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SILVERBROOK RESEARCH PTY LTD
393 DARLING STREET
BALMAIN, 2041
AUSTRALIA

EXAMINER

CHRZANOWSKI, MATTHEW R

ART UNIT

PAPER NUMBER

2186

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DELIVERY MODE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/727,157	Applicant(s) PLUNKETT, RICHARD THOMAS	
	Examiner MATTHEW R. CHRZANOWSKI	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 July 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. **Claims 1-5** rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 1-5 are non-statutory because the method claims are not tied to another category of statutory subject matter.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 1-7 and 9** rejected under 35 U.S.C. 112, first paragraph and second paragraphs, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant recites support for amendments made in claims 1 and 6, found in paragraphs [2221]-[2222] and [2294]-[2305]. The recited paragraphs show specific instances of "non-CPU" writes and the read and write requests alternating. However, the broad claim language is not shown in the cited sections, and furthermore elsewhere in the specification. The claim language, "wherein, in step (c), the earlier position is selected so as to not be adjacent a position in the list for performance of another access request of the first type" is found to be new matter. Dependent **claims 2-5, 7 and 9** inherit these defects.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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8. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. **Claims 1-5** rejected under 35 U.S.C. 103(a) as being unpatentable over **Stacovsky et al. (US Patent # 6526484 B1, hereinafter “Stacovsky”)** in view of **Non-Patent Literature (“RIOT-The Scheduling Problem,” hereinafter “NPL2”)**.

Consider **claim 1**, Stacovsky discloses a method for arbitrating between a plurality of access requests issued in relation to a resource by a plurality of requesters (*FIG. 9A-B, 14*), wherein each request can be one of at least two types, a first of the types having a higher latency associated with its performance than at least some of the other types (*it can but not necessarily does; in a system with different processors and memories it is inherent that there will be access requests of varying latencies, such as different distances between specific processors and memories, and fabrication/manufacturing defects*), the method including the steps of:

- (a) receiving a plurality of the access requests (*commands 1, 2: FIG. 14*);

(b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list (*FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue; use of FIFO memory: column 18, line 19-20; FIG. 18*); and

(c) in the event an access request is arbitrated via the lookahead pointer, initiating performance of the access request earlier than the position in the list suggests it would be performed should it be started when the current pointer reached the timeslot (*command 3 is executed before command 2, but after 1: FIG. 14*).

Stacovsky discloses the use of a FIFO and executing requests out-of-order if prioritized as discussed above, and asserts it is inherent to a FIFO to (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list. However, if the applicant references FIFO that does not maintain these pointers, Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention a First-in-first-out or ordered buffer allows (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list (*FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue*), because a use of

these buffers are a well-known way of indicating order of requests to indicate priority based on order in which the entries were received. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Stacovsky orders based on timeslot and prioritizes certain requests, however, Stacovsky may not specifically disclose prioritizing based on if the request **is of the first type** (if first type, initiate performance earlier than normal position of FIFO).

Furthermore, NPL2 discloses a system which prioritizing higher latency requests earlier than normal ordered operation (*Longest Processing Time (LPT): page 1*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to prioritizing based on if the request is of the first type in the system of Stacovsky, because NPL2 teaches the LPT is a heuristic used for finding the minimum makespan of a schedule and no one large job will "stick out" at the end of the schedule and dramatically lengthen the completion time of the last job (*page 1*). Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (*LPT scheduling algorithm*).

Furthermore, Stacovsky may not specifically disclose wherein, in step (c), the earlier position is selected so as to not be adjacent a position in the list for performance of another access request of the first type.

Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention that different types of access requests can be interleaved so as one type is not adjacent to the same type, because interleaving is a well-known concept which allows for no single type to monopolize a time period, thereby distributing evenly types in the timeslots. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Consider **claims 2**, and as applied to **claim 1** above, Stacovsky in view of NPL2 disclose the method wherein step (c) includes the substep of performing the access request indicated by the lookahead pointer immediately after the access request indicated by the current pointer is performed (*Stacovsky: command 3 is executed before command 2, but immediately after command 1: FIG. 14*).

Consider **claim 3**, and as applied to **claim 1** above, Stacovsky in view of NPL2 disclose the method wherein the first type of access request is a memory write request (*Stacovsky: column 9, lines 3-5*).

Consider **claims 4**, and as applied to **claim 3** above, Stacovsky in view of NPL2 disclose the method wherein step (c) includes the substep of performing the access request indicated by the lookahead pointer immediately after the access request indicated by the current pointer is performed (*Stacovsky: command 3 is executed before command 2, but immediately after command 1: FIG. 14*).

Consider **claim 5**, and as applied to **claim 1** above, Stacovsky in view of NPL2 disclose the method wherein the number of timeslots between the timeslot indicated by the lookahead pointer and the timeslot indicated by the current pointer takes into account a latency difference between performing an access request of the first type and at least one of the other access request types (*Stacovsky: the timeslots or entries "take into account" the latency difference because they arrive in order of receipt even though relative to time one of higher latency could have been sent before a lower latency time request but received by the arbiter afterwards; NPL2: Furthermore, takes into account priority and latency: page 1*).

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10. **Claims 6-7, and 9** rejected under 35 U.S.C. 103(a) as being unpatentable over **Stacovsky et al. (US Patent # 6526484 B1, hereinafter “Stacovsky”)** in view of **Non-Patent Literature (“RIOT-The Scheduling Problem,” hereinafter “NPL2”)** and **Radke et al. (US Patent # 6741253 B2, hereinafter “Radke”)**.

Consider **claim 6**, Stacovsky discloses an plurality of integrated circuit including: a plurality of operative units, each of which is capable of issuing a request for access to a memory accessible by the integrated circuit (*FIG. 1A, 9A-B, 14*); and an timeslot arbitrator for arbitrating between requests issued by the operative units for access to the memory (*FIG. 14*), wherein each request can be one of at least two types, a first of the types having a higher latency associated with its performance than at least some of the other types (*it can but not necessarily does; in a system with different processors and memories it is inherit that that there will be access requests of varying latencies, such as different distances between specific processors and memories, and fabrication/manufacturing defects*), the timeslot arbitrator being configured to:

(a) receiving a plurality of the access requests (*commands 1, 2: FIG. 14*);

(b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list (*FIFO and ordered buffers maintain a current pointer and future or last received pointer*

to signify the last entry in the queue; use of FIFO memory: column 18, line 19-20); and

(c) in the event an access request as arbitrated via the lookahead pointer, initiating performance of the access request earlier than the position in the list suggests it would be performed should it be started when the current pointer reached the timeslot (*command 3 is executed before command 2, but after 1: FIG. 14*).

Stacovsky discloses the use of a FIFO and executing requests out-of-order if prioritized as discussed above, and asserts it is inherent to a FIFO to (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list. However, if the applicant references FIFO that does not maintain these pointers, Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention a First-in-first-out or ordered buffer allows (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list (*FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue*), because a use of these buffers are a well-known way of indicating order of requests to indicate priority based on order in which the entries were received. Furthermore, it would have been obvious because a person of ordinary

skill has good reason to pursue the known options within his or her technical grasp.

Stacovsky orders based on timeslot and prioritizes certain requests, however, Stacovsky may not specifically disclose prioritizing based on if the request **is of the first type** (if first type, initiate performance earlier than normal position of FIFO).

Furthermore, NPL2 discloses a system which prioritizing higher latency requests earlier than normal ordered operation (*Longest Processing Time (LPT): page 1*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to prioritizing based on if the request is of the first type in the system of Stacovsky, because NPL2 teaches the LPT is a heuristic used for finding the minimum makespan of a schedule and no one large job will "stick out" at the end of the schedule and dramatically lengthen the completion time of the last job (*page 1*). Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (*LPT scheduling algorithm*).

Furthermore, Stacovsky may not specifically disclose wherein, in step (c), the earlier position is selected so as to not be adjacent a position in the list for performance of another access request of the first type.

Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention that different

types of access requests can be interleaved so as one type is not adjacent to the same type, because interleaving is a well-known concept which allows for no single type to monopolize a time period, thereby distributing evenly types in the timeslots. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Furthermore, Radke discloses placing processors and memory on an embedded/integrated circuit (*column 1, lines 14-30*).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made integrate the entire processors, memory and arbitrator in the system of Stacovsky in view of NPL2, because it is a design choice which increases throughput of processed data because the processors are closer to the memory. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Consider **claim 7**, and as applied to **claim 6** above, Stacovsky in view of NPL2 and Radke disclose the integrated circuit wherein the first type of access request is a memory write request (*Stacovsky: column 9, lines 3-5*).

Consider **claim 9**, and as applied to **claim 6** above, Stacovsky in view of NPL2 and Radke disclose the integrated circuit wherein the number of timeslots between the timeslot indicated by the lookahead pointer and the timeslot indicated by the current pointer takes into account a latency difference between performing an access request of the first type and at least one of access request types (*Stacovsky: the timeslots or entries "take into account" the latency difference because they arrive in order of receipt even though relative to time one of higher latency could have been sent before a lower latency time request but received by the arbiter afterwards; NPL2: Furthermore, takes into account priority and latency: page 1*).

Response to Arguments

11. Applicant's arguments filed 07/08/2008 have been fully considered but they are not persuasive. See above rejections and further explanation below.

12. Applicant's arguments with respect to claims 1-7 and 9 have been considered but are moot in view of the new ground(s) of rejection, necessitated by amendments to the independent claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW R. CHRZANOWSKI whose

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telephone number is (571)270-1176. The examiner can normally be reached on M-F 9am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

Matthew R Chrzanowski
Examiner
Art Unit 2186

/M. R. C./
Examiner, Art Unit 2186
8/27/2008